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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,681	08/21/2003	Ryan Lei	42P16687	1018
8791	7590 11/24/2006		EXAM	INER
	SOKOLOFF TAYLOR IIRE BOULEVARD	ISAAC, STANETTA D		
SEVENTH FLOOR			ART UNIT	PAPER NUMBER
LOS ANGELI	ES, CA 90025-1030		2812	

DATE MAILED: 11/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)				
		10/646,681	LEI ET AL.				
	Office Action Summary	Examiner	Art Unit				
		Stanetta D. Isaac	2812				
Period fo	The MAILING DATE of this communication ap or Reply	pears on the cover sheet with the	correspondence address				
WHIC - Exte after - If NO - Failu Any	ORTENED STATUTORY PERIOD FOR REPLICATION OF THE MAILING ENGINEERS IS LONGER, FROM THE MAILING ENGINEERS IN COMMENTED THE MAILING ENGINEERS IN COMMENTED THE MAILING ENGINEERS IN COMMENTED THE MAILING ENGINEERS IN COMMENT OF THE MAILING ENGINEERS I	DATE OF THIS COMMUNICATION  136(a). In no event, however, may a reply be will apply and will expire SIX (6) MONTHS from the course the application to become ABANDON	DN. timely filed m the mailing date of this communication. HED (35 U.S.C. § 133).				
Status							
1)	Responsive to communication(s) filed on 10 (	October 2006.					
2a)□		s action is non-final.					
3)	<del>/</del>						
-,	closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
Disposit	ion of Claims						
4)	Claim(s) <u>1,3,4,7,9-12,14,15,19-25,27,28,30 a</u>	nd 33-49 is/are pending in the ar	polication				
7,0	4a) Of the above claim(s) is/are withdrawn from consideration.						
5)	Claim(s) is/are allowed.						
	(i) Claim(s) 1,3,4,7,9-12,14,15,19-25,27,28,30 and 33-49 is/are rejected.						
7)	Claim(s) is/are objected to.	<u></u>					
,—		<b>1</b>					
Application Papers							
9) The specification is objected to by the Examiner.							
10) The drawing(s) filed on 21 August 2003 is/are: a) accepted or b) objected to by the Examiner.							
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).							
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.							
Priority ι	ınder 35 U.S.C. § 119						
	12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  a) All b) Some * c) None of:						
	1. Certified copies of the priority documents have been received.						
	2. Certified copies of the priority documents have been received in Application No						
	3. Copies of the certified copies of the priority documents have been received in this National Stage						
	application from the International Bureau (PCT Rule 17.2(a)).						
* 5	* See the attached detailed Office action for a list of the certified copies not received.						
		,					
Attachmen	t(s)						
1) Notice of References Cited (PTO-892)  4) Interview Summary (PTO-413)							
2) 🔲 Notic	e of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail I	Date				
	nation Disclosure Statement(s) (PTO/SB/08) r No(s)/Mail Date	5) Notice of Informal 6) Other:	Patent Application				
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Art Unit: 2812

#### **DETAILED ACTION**

This Office Action is in response to the RCE and amendment filed on 10/10/06. Currently, claims 1, 3, 4, 7, 9-12, 14, 15, 19-25, 27, 28, 30, 33-49 are pending.

#### Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/10/06 has been entered.

## Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 7, 9-12, 14, 19-25, 27, and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Reisman et al., US Patent 4,891,329.

Reisman discloses the semiconductor method as claimed. See figures 1A-1D, and corresponding text, where Reisman teaches, pertaining to claims 1, 12 and 22, a method of forming a germanium-on-insulator (GOI) substrate comprising: forming an epitaxial germanium layer 20 on top of a first substrate 10 (the epitaxial germanium layer having a rough surface, the rough surface has a roughness value approximately greater than 2nm RMS, for claim 12; figure

Art Unit: 2812

1A; col. 4, lines 21-30, *Note*: the Examiner takes the position that it is inherent the rough surface has a roughness value approximately greater than 2nm RMS, based on Applicant's admitted prior art on page 6, paragraph [0019]); forming a first dielectric film 30 on top of the epitaxial germanium layer (on top of the rough surface, for claim 12; figure 1B; col. 4, lines 30-33); providing a second semiconductor substrate 40/50 (figure 1C; col. 4, lines 54-59, *Note*: the Examiner takes the position that the second semiconductor substrate comprises both the insulating layer and the second substrate); bonding the first substrate directly to the second substrate by bonding the first dielectric film to the second substrate, the bonding resulted in a bonded wafer pair (figure 1C; col. 4, lines 60-65); and removing the first substrate after the bonding to expose epitaxial germanium layer to form the GOI substrate (and forming an electronic device on the GOI substrate, for claim 22; figure 1D; col. 4, lines 66-68; col. 5, lines 1-2; col. 6, lines 52-55).

Pertaining to claims 3, 14 and 27, Reisman teaches, a method, wherein the removing of the first substrate after the bonding includes one of a grind back process, an etching process, and an ion exfoliation process (figure 1D; col. 4, lines 66-68).

Pertaining to claims 7 and 30, Reisman teaches, a method wherein the removing of the first substrate after the bonding includes cleaving off the first substrate (figure 1D; col. 4, lines 66-68).

Pertaining to claims 9 and 19, Reisman teaches, a method wherein each of the first substrate and the second substrate semiconductor wafer is selected from a group consisting of a silicon (Si) substrate, a monocrystalline Si substrate, a polycrystalline Si substrate, a Sicontaining substrate, a Si substrate having an oxide layer, a silicon-on-insulator (SOI) substrate,

a gallium arsenide substrate, and Ge-containing substrate (col. 4, lines 22-25 and lines 54-56, both the first substrate and second substrates are silicon).

Pertaining to claims 10 and 20, Reisman teaches, a method further comprising causing a surface activation to the top surface of the first dielectric film and at least one surface of the second substrate to facilitate the bonding (col. 4, lines 60-65).

Pertaining to claims 11 and 21, Reisman teaches, a method further comprises annealing the bonded wafer pair at a predetermined annealing temperature, wherein the annealing temperature is achieved with a temperature ramp rate of approximately 1°C/minute (col. 4, lines 64-65).

Pertaining to claim 23, Reisman teaches, a method wherein the electronic device includes one of a transistor and a detector (col. 1, lines 5-12; col. 6, lines 52-55).

Pertaining to claim 24, Reisman teaches, a method wherein the transistor includes a gate dielectric, a gate electrode, spacers, and source/drain regions (col. 1, lines 5-12; col. 6, lines 52-55).

Pertaining to claim 25, Reisman teaches, a method wherein the detector includes a waveguide encapsulated by an oxide layer and at least one electrode (col.1, lines 1-12; col. 6, lines 52-55).

## Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

'Art Unit: 2812

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 15, 28, 33, 39, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reisman et al., US Patent 4,891,329 in view of admitted prior art.

Reisman disclose the semiconductor method substantially as claimed. See preceding rejection of claims 1, 3, 7, 9-12, 14, 19-25, 27, and 30 under 35 U.S.C. 102(e). In addition, Riesman shows, pertaining to claims 33, 39 and 44, a method of forming a germanium-oninsulator (GOI) substrate comprising: forming an epitaxial germanium layer 20 on top of a first substrate 10 (the epitaxial germanium layer having a rough surface, the rough surface has a roughness value approximately greater than 2nm RMS, for claim 12; figure 1A; col. 4, lines 21-30, Note: the Examiner takes the position that it is inherent the rough surface has a roughness value approximately greater than 2nm RMS, based on Applicant's admitted prior art on page 6, paragraph [0019]); forming a first dielectric film 30 on top of the epitaxial germanium layer (on top of the rough surface, for claim 12; figure 1B; col. 4, lines 30-33); providing a second semiconductor substrate 40/50 (figure 1C; col. 4, lines 54-59, Note: the Examiner takes the position that the second semiconductor substrate comprises both the insulating layer and the second substrate); bonding the first substrate directly to the second substrate by bonding the first dielectric film to the second substrate, the bonding resulted in a bonded wafer pair (figure 1C; col. 4, lines 60-65); and removing the first substrate after the bonding to expose epitaxial germanium layer to form the GOI substrate (and forming an electronic device on the GOI substrate, for claim 22; figure 1D; col. 4, lines 66-68; col. 5, lines 1-2; col. 6, lines 52-55). In addition, Riesman shows, pertaining to claims 34, 40 and 48, wherein the removing of the first substrate after the bonding includes one of a grind back process, an etching process, and an ion

Art Unit: 2812

exfoliation process (figure 1D; col. 4, lines 66-68). Also, Riesman shows, pertaining claims, 35 and 49, wherein the removing of the first substrate after the bonding includes cleaving off the first substrate (figure 1D; col. 4, lines 66-68). Riesman shows, pertaining to claims 36 and 41, wherein each of the first substrate and the second substrate semiconductor wafer is selected from a group consisting of a silicon (Si) substrate, a monocrystalline Si substrate, a polycrystalline Si substrate, a Si-containing substrate, a Si substrate having an oxide layer, a silicon-on-insulator (SOI) substrate, a gallium arsenide substrate, and Ge-containing substrate (col. 4, lines 22-25 and lines 54-56, both the first substrate and second substrates are silicon). In addition, Riesman shows, pertaining to claims 37 and 42, method further comprising causing a surface activation to the top surface of the first dielectric film and at least one surface of the second substrate to facilitate the bonding (col. 4, lines 60-65). Also, Riesman shows, pertaining to claims 38 and 43, further comprises annealing the bonded wafer pair at a predetermined annealing temperature, wherein the annealing temperature is achieved with a temperature ramp rate of approximately 1°C/minute (col. 4, lines 64-65). Riesman shows, pertaining to claim 45, wherein the electronic device includes one of a transistor and a detector (col. 1, lines 5-12; col. 6, lines 52-55). In addition, Reisman shows, pertaining to claim 46, wherein the transistor includes a gate dielectric, a gate electrode, spacers, and source/drain regions (col. 1, lines 5-12; col. 6, lines 52-55). Finally, Reisman shows, pertaining to claim, 47, wherein the detector includes a waveguide encapsulated by an oxide layer and at least one electrode (col.1, lines 1-12; col. 6, lines 52-55).

However, Reisman fails to show, pertaining to claims 4, 15, 28, 33, 39 and 44, further comprising: polishing the surface of the first dielectric film prior to the bonding.

Art Unit: 2812

On page 8, paragraph [0025], the Applicant teaches, that portions of the dielectric layer, can be removed to have a smaller thickness, where a conventional method of chemical mechanical polishing (CMP) may be used to remove some of the dielectric layer.

It would have been obvious to one of ordinary skill in the art to incorporate, a method further comprising: polishing the surface of the first dielectric film prior to the bonding, in the method of Reisman, pertaining to claims 4, 15 and 28, according to the teachings of the admitted prior art, with the motivation of, reducing the amount of dielectric material, for the purpose of creating a desired dielectric thickness.

### Response to Arguments

Applicant's arguments filed 10/10/06 have been fully considered but they are not persuasive. The Applicant raises the clear issue as to whether Riesman alone or in combination thereof, suggest bonding the insulator layer of the first substrate directly to the second semiconductor substrate.

The Examiner takes the position that Riesman does suggest bonding the insulator layer of the first substrate directly to the second semiconductor substrate. Specifically, the Applicant states, on page 10, in the second and third paragraphs, "that the bonding process is different with different interfaces", and "that the bonding between insulator and semiconductor surfaces is distinct from the bonding between two insulator surfaces". However, the limitation does not state directly to the *semiconductor surfaces* (intentionally emphasized) or any bonding process that is *different* with *different interface*" (intentionally emphasized). The claim only calls for "bonding the first substrate directly to the second substrate", where taken in its broadest interpretation, Riesman meets this limitation, by showing the step of bonding the first substrate

Application/Control Number: 10/646,681 Page 8

Art Unit: 2812

10 directly to the second substrate 40/50 (the second semiconductor substrate includes both the insulating layer and the substrate) bonding the first dielectric film 30 to the second substrate, the bonding resulted in a bonded wafer pair (figure 1C; col. 4, lines 60-65).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stanetta Isaac Patent Examiner November 21, 2006

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER